

# Triple-Slot Phase-Shifting Cell Loaded with Capacitances for Reflectarray Applications

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**Abstract**— This paper presents a new phase-shifting cell topology for reflectarray. It consists of a symmetrical set of three parallel rectangular slots loaded with a combination of variable and fixed capacitances to provide four uniformly-distributed phase states with a large bandwidth. Two different slot lengths are combined to improve the bandwidth. The cell is characterized in C-band using the waveguide simulation approach.

## I. INTRODUCTION

A reflectarray antenna consists of a set of radiating elements, called phase-shifting cells, printed on a flat surface and illuminated with a primary source (Fig. 1). The main role of each cell is to re-radiate and scatter the incident wave with a certain phase-shift required to form a specified pattern in the far-field. Reflectarrays usually use patch or slot to vary the phase of the reflected wave. By modifying the geometry of the resonant element for passive structures or its loading for active ones, the resonant frequency can be changed and so the reflected phase. One of the main challenges is to provide a phase-shifting cell with large bandwidth. For medium size reflectarrays, the bandwidth limitation is due to the dispersive nature of the resonant elements [1], [2].

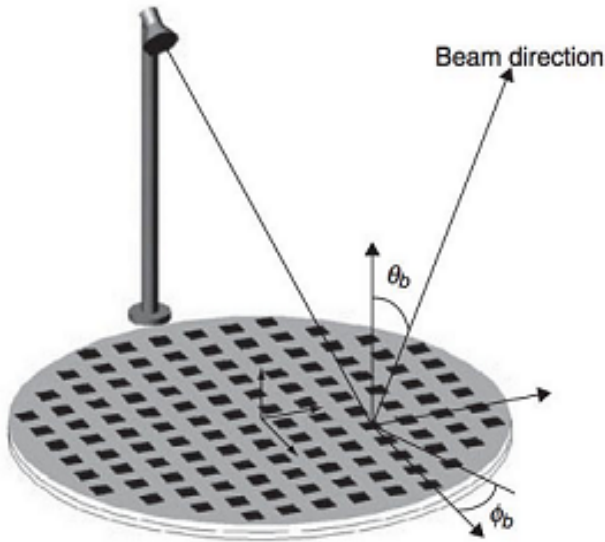


Figure 1. General reflectarray antenna configuration

Active reflectarrays are promising solutions for reconfigurable radiating apertures at reasonable cost. One of the main challenges is to design a phase-shifting cell whose phase can be controlled dynamically over a  $360^\circ$  phase range with both smooth frequency variations and low losses. MEMS are key elements for such applications due to their excellent radio-frequency (RF) properties. They are usually used as switches to control the physical length of resonating elements such as stubs, slots or rings [3-5]. Dual annular slots topologies have been demonstrated as excellent candidates to achieve passive low-loss and large bandwidth reflectarray phase-shifting cells [6]. The main object of our study is to characterize a new active cell topology with rectangular slots, loaded with a reduced number of capacitance to provide full  $360^\circ$  phase range coverage with a large bandwidth.

## II. PROPOSED PHASE-SHIFTING CELL

The proposed cell illustrated in Fig. 2 consists of a set of three parallel rectangular slots etched in a ground plane. The principle of this structure is to control the reflected phase by a single capacitance loading the central slot. The external slots are used to achieve a smooth phase evolution (and consequently a large bandwidth) as in the dual annular slot cell [6]. To do so, the resonant frequency of these external slots has to be optimized. Here, this is done by loading the external slots with a fixed capacitance  $C_1$ . Indeed, this capacitance increases the electrical length of the slots [7] with no need to bend them (as in the annular slot) or to raise cell size.

The performances of the proposed topology have been assessed at 5.35GHz. Numerical characterizations with HFSS® have been carried out. The cell is  $35 \times 35 \text{ mm}^2$  large and is printed on a substrate with 2.17 dielectric constant and 1.6 mm thickness (Fig. 2). It is suspended 15.7mm above a square metallic cavity (Fig. 3). In the following simulations, for simplicity, all capacitances are assumed to be gap capacitances whose value can be tuned by choosing the electrode's length ( $L$  in Fig. 2). We remind that, at the end of the optimizing process,  $C_1$  will be a fixed capacitance while  $C_2$  will be a variable one (possibly representing a MEMS). As a preliminary step, four "frozen" values of  $C_2$  will be chosen to demonstrate a 2-bit phase-shifting cell with large bandwidth on a single substrate layer.

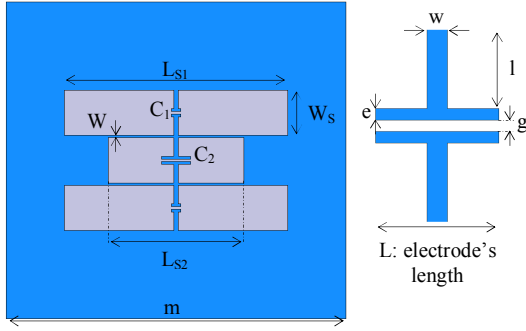


Figure 2. Characterized Phase-Shifting cell ( $L_{S1}=23\text{mm}$ ,  $L_{S2}=11\text{mm}$ ,  $W_s=5\text{mm}$ ,  $W=0.2\text{mm}$ ,  $m=35\text{mm}$ ,  $w=0.5\text{mm}$ ,  $e=0.2\text{mm}$ ,  $g=0.2\text{mm}$ ,  $l=2.2\text{mm}$ ,  $L=1\text{mm}$  for external slots,  $L=\{0.6, 2.55, 3.45, 5.6\}\text{mm}$  for central slot)

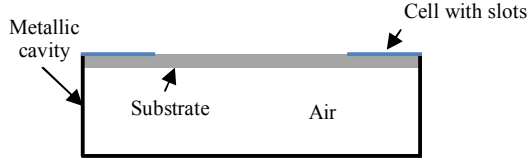


Figure 3. Side view of the cell with the metallic cavity

The synthesis of the cell is carried out as follows. Firstly, the initial dimensions of the cell (especially  $L_{S1}$ ) are optimized under normal incidence in a way to get at least  $270^\circ$  phase range without any capacitance in the central slot when its length is varied. Indeed, increasing the length  $L_{S2}$  of the central slot pushes the phase responses to lower frequencies and increases the phase range provided by the cell (Fig. 4). Thus four uniformly-distributed phase states can be selected at the central frequency in order to obtain a 2-bit phase-shifter. Secondly, the four identified values of  $L_{S2}$  are synthesized by using an appropriate loading of a fixed central slot, i.e. by varying  $L$ . As an illustration, the phase responses and the losses for the four selected capacitance values are presented in Fig. 5 and 6. We note a uniform distribution of the four phase states at  $5.35\text{GHz}$  with linear and parallel variations of the phase versus frequency; furthermore, the losses are less than  $0.15\text{dB}$ .

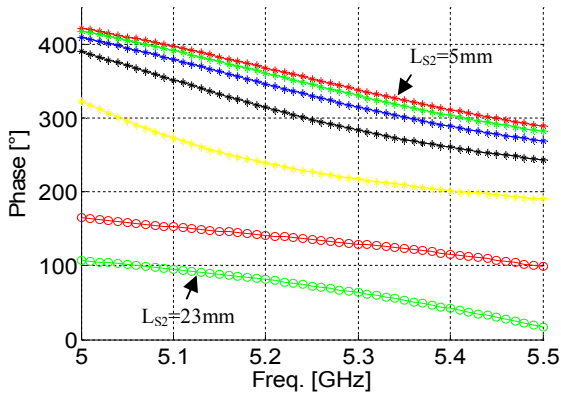


Figure 4. Phase responses versus frequency when  $L_{S1}=23\text{mm}$ ,  $L_{S2}$  is varied from  $5\text{mm}$  to  $23\text{mm}$

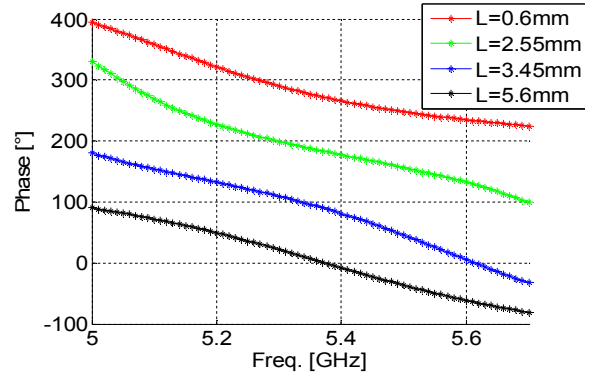


Figure 5. Four selected phase responses for different values of  $L$ , when  $L_{S1}=23\text{mm}$ ,  $L_{S2}=11\text{mm}$

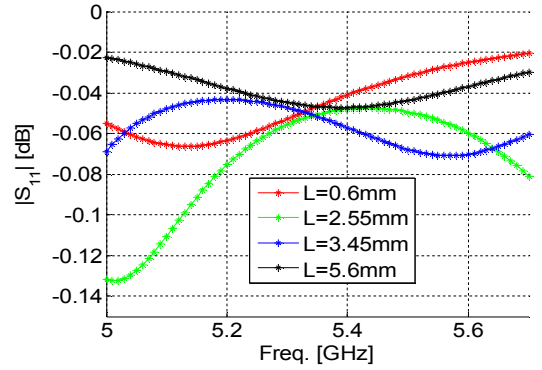


Figure 6. Losses for the four selected phase responses

Fig. 7 illustrates the variation of the phase standard deviation versus frequency. As shown in [8], the standard deviation is  $26^\circ$  for an ideal 2-bit phase-shifter. Here, we define the bandwidth as the frequency range for which the standard deviation remains below  $31^\circ$  which is better than a 1.74-bit phase-shifter. The achieved bandwidth is consequently 12% (from  $5.02\text{GHz}$  to  $5.66\text{GHz}$ ). Furthermore, the stability of the phase standard deviation (close to the ideal  $26^\circ$  value over a large bandwidth) reflects the parallelism of the phase responses versus frequency as seen in Fig. 5.

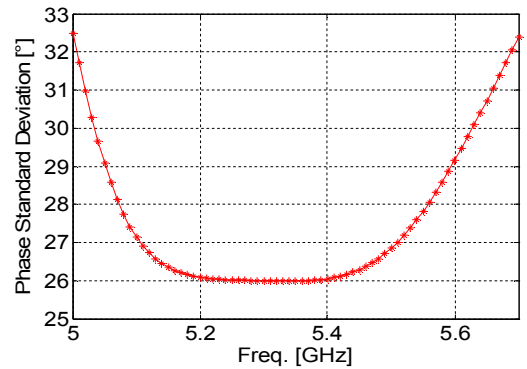


Figure 7. Phase Standard deviation versus frequency

### III. WAVEGUIDE SIMULATION APPROACH

In order to initiate an experimental characterization, the 4 selected configurations of the cell are now simulated using the waveguide approach by placing the cell at the end of a  $35 \times 35 \text{ mm}^2$  square metallic waveguide. This specific configuration corresponds to a  $53^\circ$  incidence of the impinging wave instead of the normal incidence which has been assumed in the design process, due to the reflection of the wave on the walls of the waveguide. The behavior of each of the four configurations in the waveguide, in comparison to the behavior obtained under normal incidence, is shown in Fig. 8. The phase responses are shifted to lower frequencies without any modification in the operation mode of the cell. The new phase standard deviation versus frequency is illustrated in Fig. 9; it shows that the bandwidth is reduced to 10.5% (from 4.87GHz to 5.41GHz).

Four different layouts were fabricated, each of which corresponds to one of the selected capacitances, and measured in a C band metallic waveguide. Fig. 10 shows that the agreement between measurements and simulations for the phase standard deviation is very good. Unfortunately, measurements could only be done from 5GHz as the waveguide cutoff frequency is 4.28 GHz and a nearly 20% margin was used to prevent from high dispersion near cutoff. As a result, experimental performance can not be assessed accurately below 5.1GHz.

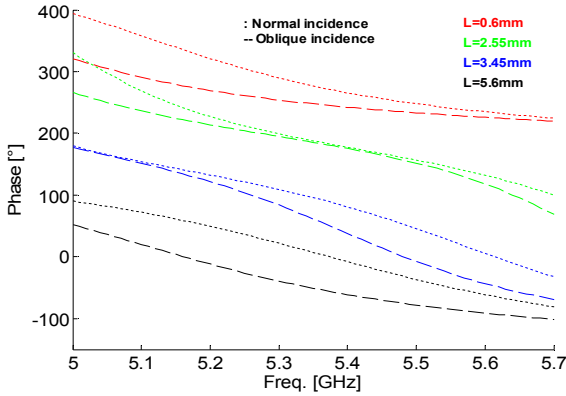


Figure 8. Phase responses for different values of L for normal and oblique incidences

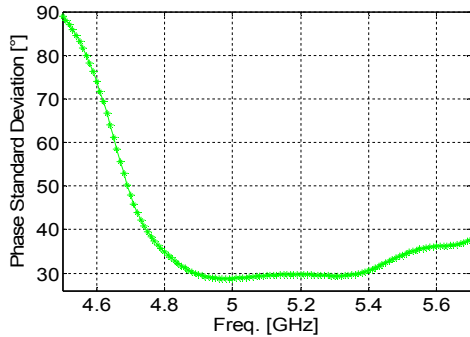


Figure 9. Phase standard deviation for waveguide simulation

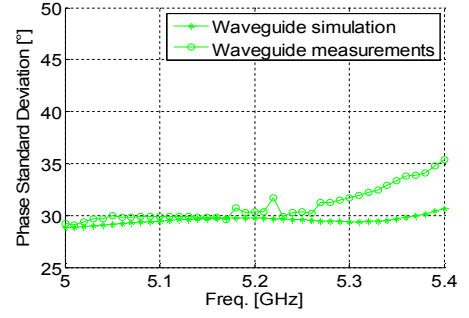


Figure 10. Comparison between simulation and measurements for the phase standard deviation

### IV. INCIDENCE'S EFFECT ADJUSTMENT

In order to respect the constraint of 20% margin above the cutoff frequency of the waveguide and to provide a useful operating band beyond 5GHz, the two slots were resized, the new optimized lengths are 10mm and 21mm for  $L_{S2}$  and  $L_{S1}$  respectively. In addition, to improve further the performances of the waveguide configuration, it is essential to correct the effect of the incidence on the phase responses. To do so, the electrode's length L of the central capacitance was then optimized directly in the waveguide simulations. The four suitable values of L are now respectively 0.8mm, 2.9mm, 3.71mm and 5.5mm. (instead of the values optimized for normal incidence as given in Fig. 5). As it is shown in Fig. 11, 12 and 13 respectively, these new values provide a uniformly distributed phase states at 5.35GHz, losses lower than 0.2dB and a 11.5% bandwidth (from 5.08GHz to 5.7GHz).

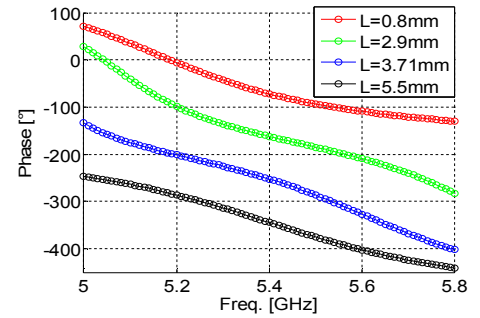


Figure 11. Four selected phase responses provided by the cell in the metallic waveguide for  $L_{S1}=21\text{mm}$ ,  $L_{S2}=10\text{mm}$

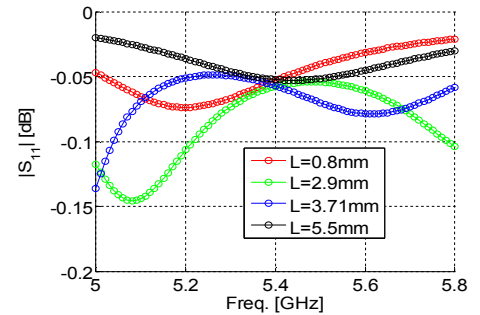


Figure 12. Losses for the new selected phase responses

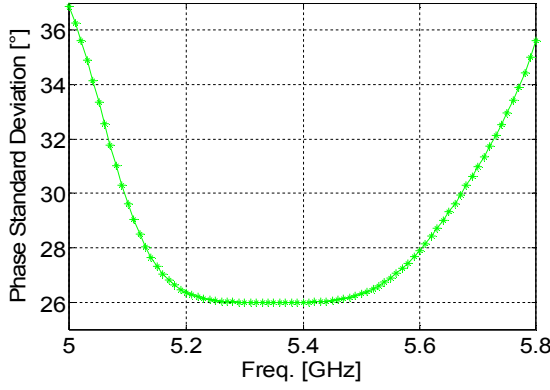


Figure 13. New phase standard deviation versus frequency

## V. CAPACITIVE MEMS SWITCHES

In order to provide a dynamical control of the cell, capacitive MEMS switches should replace the gap capacitance in the central slot. We remind that the loading in the external slots involves a fixed capacitance (used to improve compactness) which means no MEMS are required there. The first column of Table I summarizes the four required values of  $C_2$  (corresponding to Fig. 11). Using typical values of MEMS capacitance, i.e.  $C_{up}=20\text{fF}$  and  $C_{down}=400\text{fF}$  [9], the four required values of  $C_2$  could be realized with 2 series MEMS and two shunt fixed capacitances as illustrated in Fig. 14. Table I shows the possible combinations.

TABLE I. EQUIVALENT CAPACITANCE FOR DIFFERENT MEMS STATES

$C_2$	MEMS1	MEMS2	$C_{\text{fixed1}}$	$C_{\text{fixed2}}$
36fF	20fF	20fF	70fF	40fF
53fF	400fF	20fF	70fF	40fF
74fF	20fF	400fF	70fF	40fF
227fF	400fF	400fF	70fF	40fF

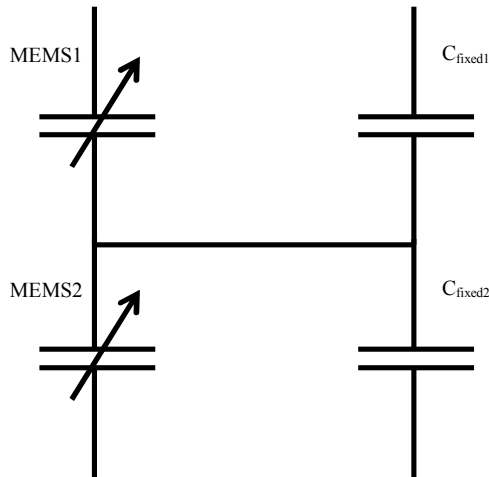


Figure 14. Loading configuration of the central slot to synthesize  $C_2$

By doing so, this type of cell loaded with only 2 capacitive MEMS switches can provide an efficient phase shifter (4 uniformly distributed phase states) with low losses and a large bandwidth.

## VI. CONCLUSION

A new triple-slot phase-shifting cell has been designed. By varying the capacitive loading of the central slot only, a large phase range with quite linear variations versus frequency can be obtained. In the present communication, a fixed capacitive loading of the external slots has also been used to improve the overall compactness of the cell. As a potential application for reconfigurable reflectarrays, a 1.74-bit phase-shifting cell has been demonstrated in C-band. It only requires 4 different values of the loading capacitance which could be achieved with only two capacitive MEMS in switching mode. The theoretical bandwidth reaches 11.5% with losses lower than 0.2 dB. Four different layouts were fabricated and measures in a C-band metallic waveguide, experimental results are in quite good agreement with simulations and confirm the potentialities of the proposed cell.

## ACKNOWLEDGMENT

This study was carried out within the French R3MEMS ANR project.

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